



Asynchronous design demonstrated at 130nm

By Ron Wilson
March 6, 2003

SAN MATEO, Calif. — Fulcrum Microsystems (Calabasas Hills, Calif.), has reported successful characterization of a 130 nm test chip carrying its fully asynchronous Nexus crossbar switch block.

The design was taped out for TSMC's 130 nm lp process and run on a standard cybershuttle. Fulcrum received 400 dice, giving them a sufficient number for statistical data as well as proof of concept.

Robert Nunn, Fulcrum's president and chief executive, said the lot revealed that the asynchronous design behaved precisely as predicted, operating over a wide range of temperature and supply voltage, and producing excellent operating speed: 1.4 GHz at the 1.2V process center, with measured performance up to 1.6 GHz at 1.4V.

Fulcrum's architecture is based on a two-wire, self-timed logic library in which each logic signal has three states: true, false and not ready. Signals propagate through the logic at their own rate, rather than moving from register to register in response to a clock signal. A logic function only operates when all of its inputs have shifted out of the "not ready" state.

This behavior, in theory, should have a number of important benefits. It should permit a chip to operate at exactly the speed of its critical timing path, independent of temperature, voltage and even, Nunn pointed out, delay faults on the die. This should permit a self-timed design both to operate at a higher speed in a given process and to produce better yields compared to a synchronous design.

In fact the operating characteristics measured on the 130 nm dice supported that theory, according to Nunn. Operating frequency varied smoothly with power without any need to screen circuits for a maximum clock frequency.

At nominal conditions the crossbar module substantially outperformed synchronous designs of similar complexity. Further, since the self-timed circuitry is automatically quiescent unless valid logic levels are propagating through it, active current varies linearly with activity, rather than with clock frequency.

The test dice consumed under 4W at 1.2V, while carrying an aggregate data throughput of 800 Gb/s.