

## Product Brief

## Six-Interface SPI-4.2 Interconnect

The PivotPoint FM1010 System Interconnect is a high-performance solution for seamlessly and intelligently interconnecting multiple chips with SPI-4.2 interfaces, enabling designers to deliver sophisticated systems while significantly reducing costs, increasing system flexibility, and reducing time to market. At the heart of the PivotPoint family is a compact, high-performance non-blocking crossbar that offers sustained per-port throughput of 32 Gbps (duplex), low end-to-end latency, and several reconfiguration and dynamic switching modes. The PivotPoint FM1010 converts a fixed-configuration half-duplex daisy-chain of devices with SPI-4 interfaces (such as NPUs, traffic managers, co-processors, search engines, custom ASICs, and FPGAs) into a dynamically-reconfigurable full-duplex resource pool, enabling more efficient use of the silicon resources, and eliminating the custom glue logic that often accompanies complex system designs. (Also available for lower-density applications is the FM1020 three-interface SPI-4.2 interconnect.)

### Features

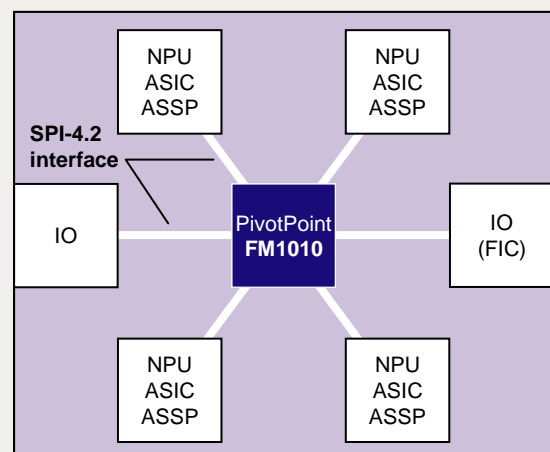
- **Six SPI-4 Phase 2 packet interfaces**
  - Complies with OIF Implementation Agreement
  - Each independently clocked up to 450 MHz
  - Implements LVTTTL status channel
  - Configurable de-skew (fully dynamic, or static)
  - Full-duplex operation up to 14.4 Gbps per interface
  - Up to 256 ports (channels) per interface
  - Enables glueless interconnection of compatible devices
- **32KB packet buffers per interface**
  - 16KB ingress buffer (minimum of 1KB per port)
  - 16KB egress buffer (minimum of 1KB per port)
  - Configurable to support a single stream or multiple ports
- **Nexus<sup>™</sup> High Capacity System Interconnect**
  - Asynchronous design enables seamless interconnection of interfaces operating at disparate data rates
  - Six independent non-blocking ports
  - 32 Gbps internal capacity per port per direction
  - Implements work-preserving round-robin fair arbitration
- **Low latency**
  - <3ns through crossbar (including link establishment)
  - <250ns end to end (including link establishment)
- **Soft-configurable operating modes**
  - Configurable static interface mapping (any-to-any)
  - Configurable static port mapping
  - Modes can be mixed for greater flexibility
- **16-bit processor interface**
  - Provides glueless connection to the local control CPU
- **JTAG test interface**
  - Provides boundary scan for production test
  - Enables system-level debug from a central location
  - Provides access to internal configuration tables
- **Built-in flow control**
  - Fulcrum delay-insensitive logic automatically propagates back-pressure on congestion or starvation
- **Modest and flexible power profile**
  - < 2.5W per active interface
  - Power scales linearly on activity

### Benefits

- **Transparent interconnection**
  - An intelligent combination of significant over-speed, large configurable buffers, and work-preserving fair arbitration helps eliminate contention and jitter in the system
- **Improved system configuration flexibility**
  - Configurable modes for either static mapping or dynamic switching increases system flexibility while preserving deterministic behavior for mission-critical applications
- **Increased system debug flexibility**
  - JTAG interface and internal serial tree enable direct access to all interconnected devices
- **Increased system design efficiency**
  - Eliminates the cost, development time, and high power profile of traditional FPGA "glue logic"

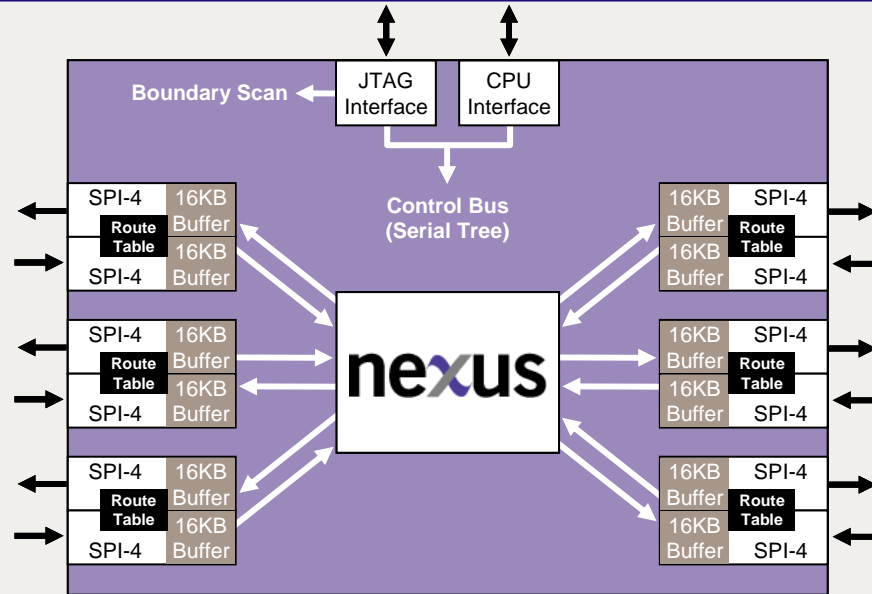
### Sample Application

#### Multi-Service Line Card



*The PivotPoint FM1010 simplifies system design, while improving performance and configuration flexibility, and reducing component cost, system power, and time to market. The PivotPoint FM1010 enables system silicon to be addressed as shared resources, rather than discrete, hard-connected devices.*

## Block Diagram



*Leveraging the unique capabilities of Fulcrum's Nexus System Interconnect, the PivotPoint FM1010 delivers vast throughput with negligible delays. Links can be established, and channels arbitrated, at full SPI-4.2 interface line rate – sustained.*

## Improving System Flexibility

As the industry converges on SPI-4.2 for reliable high-speed chip-to-chip interconnection, devices are emerging with a variety of capabilities – from packet processing, to security co-processing, to policy management, and port aggregation. As a result, system designers are now able to gluelessly interconnect standard devices to create high-speed systems while reducing complexity and cost. With the addition of the PivotPoint FM1010, designers gain flexibility and performance advantages unavailable with discrete daisy-chain designs by linking chips together in a reconfigurable fashion and treating them as shared resources that can be dynamically allocated as needed.

The PivotPoint FM1010 can provide interconnection between as many as six full-duplex SPI-4.2 devices, using any relevant combination of the following methods:

- **Configurable static interface mapping.** Any ingress interface can be static-mapped to any egress.
- **Configurable static port mapping.** Any port on any ingress interface can be statically mapped to any port on any egress interface.
- **Source routing to any interface or port.** A connected device can intelligently allocate traffic to ports, and PivotPoint can switch based on the port IDs.

## Easing System Design

The PivotPoint FM1010 provides a seamless and nearly-transparent infrastructure for efficiently interconnecting multiple SPI-4.2 devices, enabling system designers to rapidly assemble complex silicon systems. As the central nervous system, the PivotPoint FM1010 contains advanced test capabilities (including a serial tree that provides central access to all connected devices, built-in vector-based test engine that facilitates at-speed testing, JTAG boundary scan, and per-interface loop back) that combine to ease system bring-up, debug, and test.

## Process, Package, and Power

The PivotPoint FM1010 is implemented in TSMC's 130nm FSG process and is available in a 1232-ball BGA package.

By combining Fulcrum's delay-insensitive logic with aggressive interface gating, the PivotPoint FM1010 consumes power linearly and predictably based on activity and number of active interfaces.

PivotPoint consumes less than 12 Watts typically. Maximum power for configurations with fewer active interfaces is approximately 2.5 Watts per active interface.



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